Name and Std ID: Wyatt Duberstein 629635057 Lab Section: 19

Date: 10/26/2020

**PRELAB:**

**Q1.** Read section 2.2 and write the Verilog code for a 4-to-1 multiplexer.

module m4to1(W0, W1, W2, W3, S, F);

input W0, W1, W2, W3;

input [1:0] S;

output F;

always @(W0 or W1 or W2 or W3)

begin

case ({W0,W1,W2,W3})

2'b00: F = W0;

2'b01: F = W1;

2'b10: F = W2;

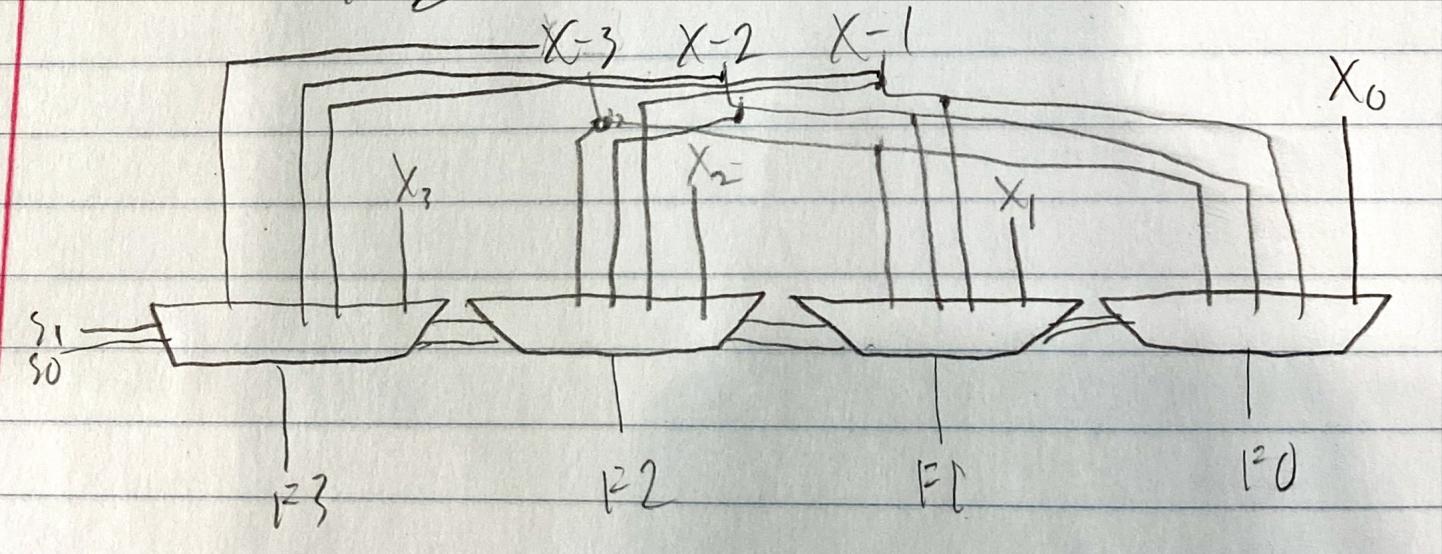
2'b11: F = W3;

endcase

end

endmodule

**Q2.** Design a 4-bit shifter as described in Section 3.1 of the lab description. Sketch the block diagram for your design showing the multiplexers, the inputs, outputs and the selectors to each multiplexer.



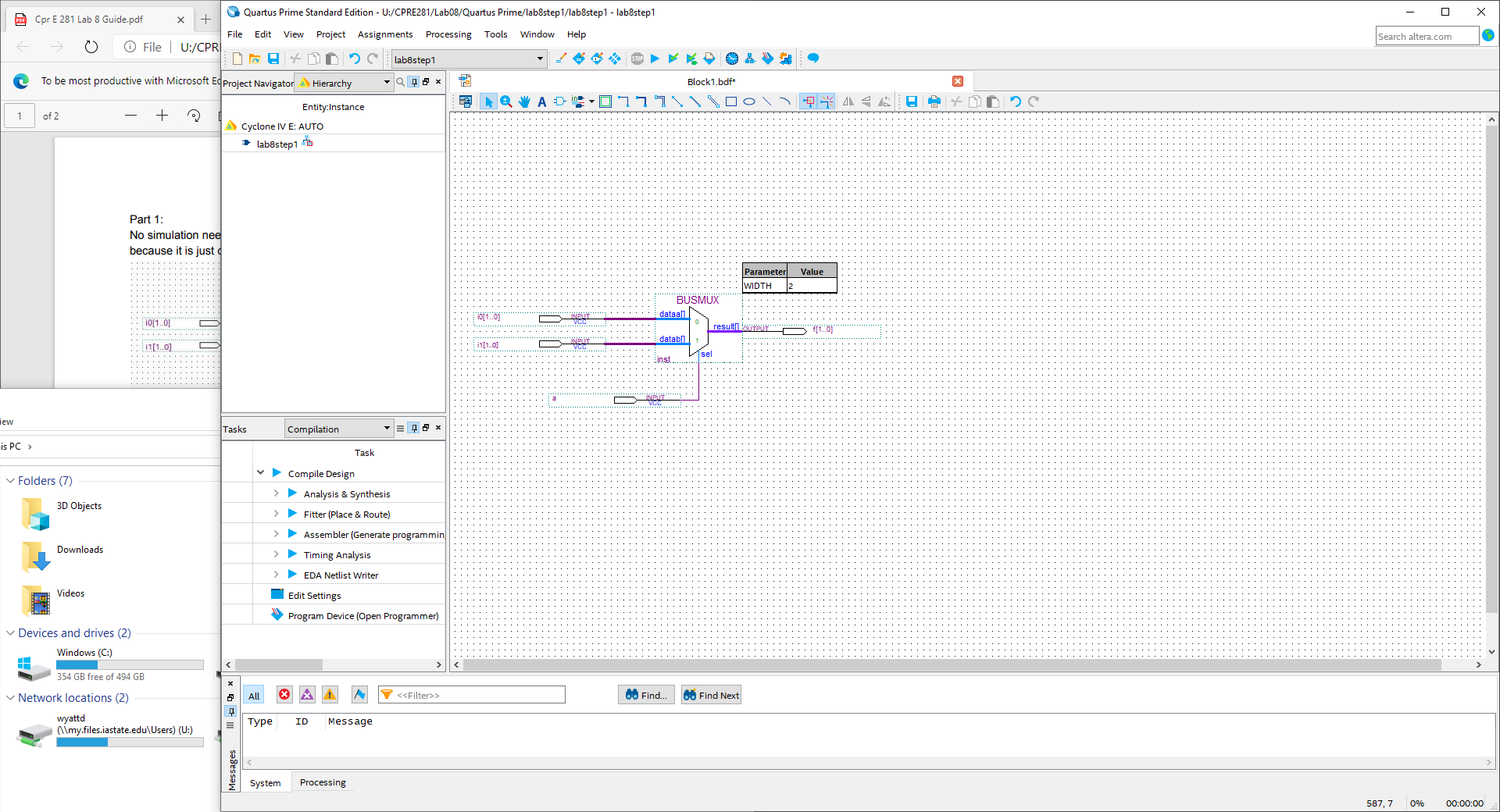
**Q3.** Refer to Section 3.1 of the lab description and complete the following table before you come to the lab:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **X3** | **X2** | **X1** | **X0** | **X-1** | **X-2** | **X-3** | **S1** | **S0** | **F3** | **F2** | **F1** | **F0** |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |

**LAB:**

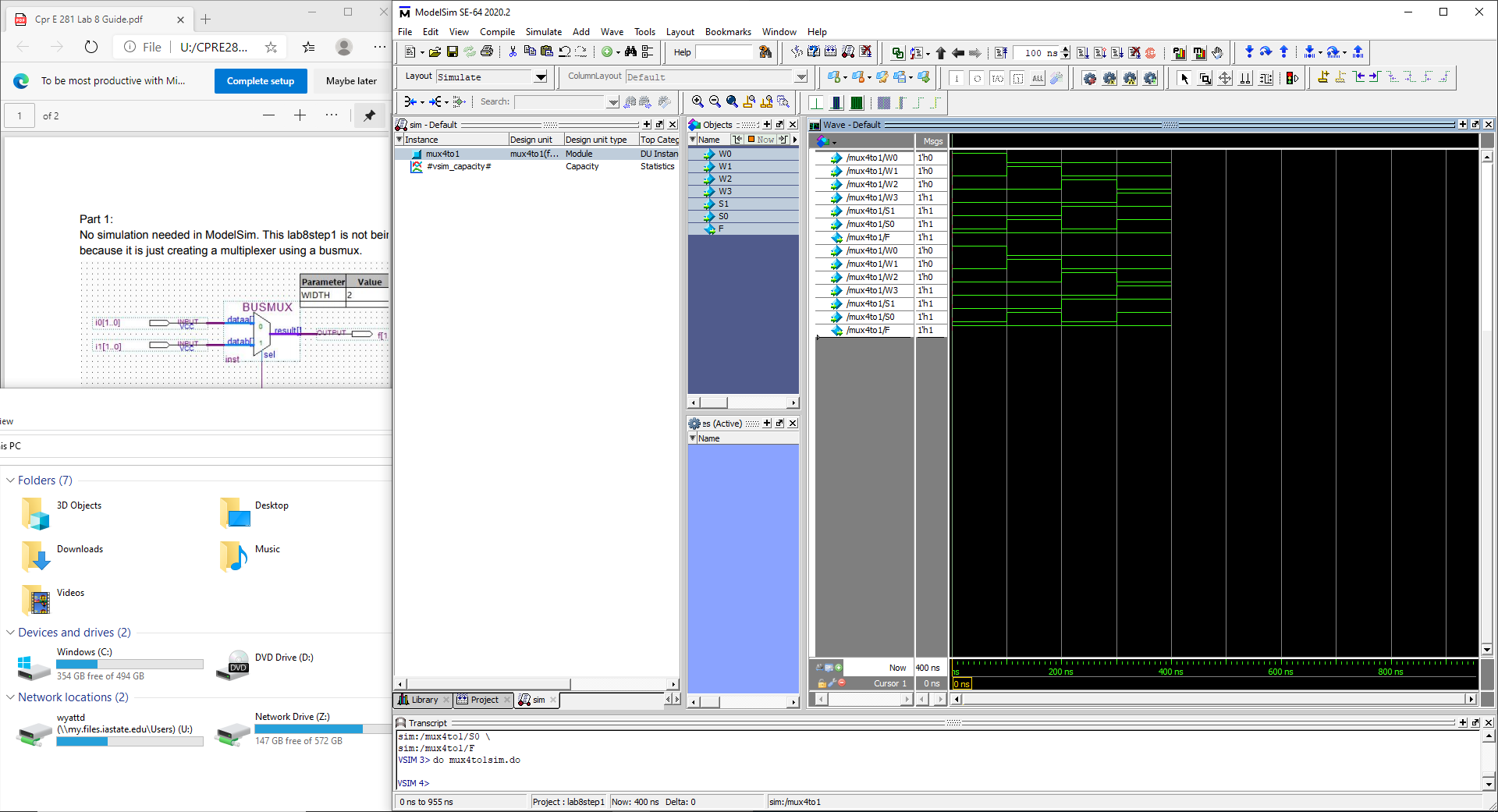
**2.1**  Hardware results demonstrate a good circuit.

Screenshots:



**2.2**  Hardware results demonstrate correct code.

Screenshots:



**3.1**  Hardware results demonstrate correct code.

Screenshots:

